

In the claims:

For the Examiner's convenience, all pending claims are presented below.

- 1 1. (Original) A system comprising:
2 a first integrated circuit (IC);
3 an interface coupled to the first IC; and
4 a second IC coupled to the interface, wherein the first IC simultaneously transmits
5 the state of each of a plurality of signals not associated with the interface to the second IC
6 in-band via the interface each time that a change in the state of one of the plurality of
7 signals is detected.
- 1 2. (Original) The system of claim 1 wherein the state of all of the plurality of
2 signals is sampled at the first IC whenever any of the signals change.
- 1 3. (Original) The system of claim 1 wherein the second IC drives each of the
2 signals with new values received in-band each time that the plurality of signal values are
3 received.
- 1 4. (Original) The system of claim 1 wherein the first IC comprises:
2 signal logic associated with each of the plurality of signals; and
3 protocol logic, coupled to the signal logic associated with each of the signals, to
4 transmit the signal values in-band to the protocol to the second IC.
- 1 5. (Original) The system of claim 4 wherein the signal logic includes:

2 a first flip-flop with an input coupled to an associated signal and an output
3 coupled to the protocol logic, the output of the first flip-flop generating a held signal
4 value; and
5 a second flip-flop having an input coupled to the output of the first flip-flop to
6 receive the held signal value, the output of the second flip-flop generating a send signal.

1 6. (Original) The system of claim 4 wherein the signal logic includes:
2 a flip-flop with an input coupled to an associated signal and an output coupled to
3 the protocol logic, the output of the flip-flop generating a held signal value; and
4 a counter having an input coupled to the output of the flip-flop to receive the held
5 signal value, the output of the second flip-flop generating a send signal.

1 7. (Original) The system of claim 4 wherein the protocol logic selects a protocol
2 point including all of the held signal values simultaneously and integrates the protocol
3 point into a protocol that is transmitted to the second IC via the interface.

1 8. (Original) The system of claim 7 wherein the protocol point being transmitted
2 is changed each time an additional signal transitions so that subsequent signal transitions
3 are communicated with a short a latency.

1 9. (Original) The system of claim 1 wherein signal transitions that occur to close
2 to previous transitions to be repeated between the first IC and the second IC via the
3 interface are discarded and more widely spaced transitions and the steady-state value of
4 the signals is repeated.

1 10. (Original) The system of claim 1 wherein the second IC comprises:
2 protocol logic, coupled to the interface, to receive each of the in-band signals and
3 to extract the state of each of the in-band signals; and
4 sequential logic, coupled to the protocol logic, to maintain the state of each of the
5 in-band signals once the state has been received.

1 11. (Original) A method comprising:
2 monitoring the state of each of a plurality of signals at a first integrated circuit
3 (IC); and
4 transmitting the state of each of the plurality of signals in-band across an interface
5 to a second IC each time that a change in the state of one of the plurality of signals is
6 detected.

1 12. (Original) The method of claim 11 wherein monitoring the state of each of a
2 plurality of signals at the first IC comprises:
3 monitoring a signal held value at protocol logic associated with each of the
4 plurality of signals; and
5 monitoring a send signal at the protocol logic associated with all of the plurality
6 of signals.

1 13. (Original) The method of claim 12 further comprising:
2 selecting a protocol point including all of the held values of the input signals
3 simultaneously at the protocol logic: and

4 integrating the protocol point into a protocol that is transmitted to the second IC
5 via the interface.

1 14. (Original) The method of claim 13 further comprising:
2 receiving the protocol point at the second IC; and
3 extracting the state of each of the plurality of in-band signals.

1 15. (Original) A system comprising:
2 a chipset;
3 an interface coupled to the chipset; and
4 an integrated circuit (IC) coupled to the chipset, wherein the chipset
5 simultaneously transmits the state of each of a plurality of signals not associated with the
6 interface to the IC in-band via the interface each time that a change in the state of one of
7 the plurality of signals is detected.

1 16. (Original) The system of claim 15 wherein the state of all of the plurality of
2 signals is sampled at the chipset whenever any of the signals change.

1 17. (Original) The system of claim 15 wherein the IC drives each of the signals
2 with new values received in-band each time that the plurality of signal values are
3 received.

1 18. (Original) The system of claim 15 wherein the chipset comprises:
2 signal logic associated with each of the plurality of signals; and

protocol logic, coupled to the signal logic associated with each of the signals, to transmit the signal values in-band to the protocol to the IC.

19. (Original) The system of claim 18 wherein the signal logic includes:

a first flip-flop with an input coupled to an associated signal and an output coupled to the protocol logic, the output of the first flip-flop generating a held signal value; and

a second flip-flop having an input coupled to the output of the first flip-flop to receive the held signal value, the output of the second flip-flop generating a send signal.

20. (Original) The system of claim 18 wherein the signal logic includes:

a flip-flop with an input coupled to an associated signal and an output coupled to the protocol logic, the output of the flip-flop generating a held signal value; and

a counter having an input coupled to the output of the flip-flop to receive the held signal value, the output of the counter generating a send signal.

21. (Original) The system of claim 18 wherein the protocol logic selects a

protocol point including all of the held signal values simultaneously and integrates the protocol point into a protocol that is transmitted to the IC via the interface.

22. (Original) The system of claim 21 wherein the protocol point being

transmitted is changed each time a held signal transitions so that subsequent signal transitions are communicated with a short a latency.

1 23. (Original) The system of claim 15 wherein signal transitions that occur to
2 close to previous transitions to be repeated between the chipset and the IC via the
3 interface are discarded and more widely spaced transitions and the steady-state value of
4 the signals is repeated.

1 24. (Original) The system of claim 15 wherein the IC comprises:
2 protocol logic, coupled to the interface, to receive each of the in-band signals and
3 to extract the state of each of the in-band signals; and
4 sequential logic, coupled to the protocol logic, to maintain the state of each of the
5 in-band signals once the state has been received.